

TITLE OF THE INVENTION

DATA PROCESSING APPARATUS AND DATA TRANSFER CONTROL
METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application is based upon and claims the
benefit of priority from the prior Japanese Patent
Application No. 11-238775, filed August 25, 1999, the
entire contents of which are incorporated herein by
reference.

10 BACKGROUND OF THE INVENTION

 The present invention relates to a data processing
apparatus and a data transfer control method thereof
and, more particularly, to a data processing apparatus
for processing various kinds of data, such as
15 audio/video data, other data and programs, and a data
transfer control method thereof.

 Recently, as the computer technology is advancing,
various types of digital information device, such as
multimedia-handling personal computers, set-top boxes,
20 digital TVs and game machines, have been developed.
There has been a demand for a capability to handle
various kinds of media, such as broadcasting media,
communication media and storage media, in digital
information devices of this type.

25 Accordingly, people are demanding that personal
computers should be provided with a function of
processing AV (Audio/Video) stream data that needs

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bus. In a case of handling streams of a variable bit rate, such as DVD titles, it was necessary to install a large buffer so that the buffer on a reception-side device would not overflow even at the maximum transfer rate. This requirement is a big factor to increase the cost. In order to multi-cast AV stream data to a plurality of devices, a huge buffer has to be provided at every device on the receiver side. This increases the cost greatly.

Furthermore, if priority is given only to the transfer of AV stream data, when an event which needs fast processing occurs, a process for that event may be delayed.

Conventional AV machines physically accomplish peer-to-peer connection of devices that handle AV streams by connecting a plurality of devices in the processing order of the AV streams. Therefore, in conventional AV machine, AV streams are not basically input to a CPU. The recent appearance of media (hyper media), which has AV streams and interactive commands integrated, demands that a CPU should process streams. This makes the present physical peer-to-peer connection of devices difficult, and studies on bus connection have started.

BRIEF SUMMARY OF THE INVENTION

An object of the present invention is to provide a data processing apparatus capable of an efficient

multi-cast transfer of stream data through a bus without providing any huge buffer, and a data transfer control method of the data processing apparatus.

To attain the above object, a data processing apparatus according to the present invention comprises a bus for which a band-guaranteed cycle capable of transferring stream data in real time by assigning a predetermined reserved band for each cycle time is defined, a plurality of nodes connected to the bus and capable of transmitting/receiving stream data using the band-guaranteed cycle, means for executing a multi-cast transfer of stream data from a sender node to a plurality of receiver nodes using the band-guaranteed cycle, and means for detecting that any of the plurality of receiver nodes drives a signal line in the bus, which indicates a completion of a data transfer cycle; and means for stopping the multi-cast transfer upon detection of the detecting means.

In the above arrangement, too, the problem of a drive conflict among signals of the plural receiver nodes can be resolved without decreasing the bus use efficiency.

According to the system of the present embodiment described above, the use of the bus in which the band-guaranteed cycle is (defined) as a transfer mode allows the band of stream data requiring a high degree of real time to be guaranteed. Usually data transfer cannot be

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intermitted during the band-guaranteed cycle; however, in the present invention, the transmission of stream data from the sender node can be stopped under the control of the receiver node, even during the band-guaranteed cycle.

The multi-cast transfer using the band-guaranteed cycle can be stopped even in response to an instruction from any receiver node. The provision of this scheme of stopping the multi-cast transfer of stream data under the control of the receiver node can prevent the buffer from overflowing even when such overflowing is likely to occur at any receiver node for the multi-cast due to a delay in the stream processing and reception of a variable bit rate stream. It is therefore possible to efficiently execute the multi-cast transfer of stream data through the bus only with the least required buffer.

When the signal line for indicating the completion of a data transfer cycle is so formed that it can be driven by any receiver node, if a drive conflict occurs among signals of the plural receiver nodes, the signal line is set in an unstable state between low and high levels, thus causing the device to malfunction. Therefore, a pull-up or pull-down load circuit is connected to the signal line, and it is preferable that an operation for driving the signal line into the active state be performed through an output buffer

provided at each receiver node. The above problem can thus be resolved. Since, in this case, a shift of the signal line from the active state to the inactive state is performed by the load circuit, a relatively long
5 time is required and accordingly an operator therefore has to wait a long time until the transfer of data is started through the multimedia bus, and it is likely that bus use efficiency will be reduced. It is therefore preferable to further comprise acceleration
10 means for driving the signal line into an inactive state for a predetermined time period after the signal line is driven into the active state by the receiver node in order to accelerate a shift of the signal line to the inactive state. If the acceleration means is
15 provided at the manager node to allow it to drive the signal line into the inactive state, the operation can be increased further in reliability.

Additional objects and advantages of the invention will be set forth in the description which follows, and
20 in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

25 BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification,

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illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. 1 is a block diagram illustrating the configuration of a system of a data processing apparatus according to one embodiment of the present invention;

FIG. 2 is a diagram for explaining cycle time used in a multimedia bus of the system according to the embodiment;

FIG. 3 is a diagram for explaining a stream access which is used in the multimedia bus according to the embodiment;

FIG. 4 is a diagram showing a channel control register used in the system of the embodiment;

FIGS. 5A and 5B are diagrams for explaining the principle of reserved band cycle flow control which is used in the embodiment;

FIG. 6 is a timing chart showing specific timing for the flow control in FIGS. 5A and 5B;

FIGS. 7A and 7B are diagrams exemplifying a hardware structure which accomplishes the flow control in FIGS. 5A and 5B;

FIG. 8 is a diagram depicting the structure of a channel detecting section provided for each node in the

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embodiment;

FIG. 9 is a diagram showing a circuit arrangement of circuits around a disconnect signal line used for the flow control shown in FIGS. 5A and 5B;

5 FIG. 10 is a timing chart showing an example of timing of the disconnect signal line at the time of flow control used in the embodiment;

FIG. 11 is a timing chart showing another example of timing of the disconnect signal line at the time of flow control used in the embodiment; and

10 FIG. 12 is a block diagram showing an example of the hardware structure for achieving the timing of FIG. 11.

DETAILED DESCRIPTION OF THE INVENTION

15 An embodiment of the present invention will now be described with reference to the accompanying drawings.

FIG. 1 illustrates the system configuration of a data processing apparatus according to one embodiment of the present invention. This data processing

20 apparatus is a multimedia-handling computer capable of handling various kinds of media, such as broadcasting media, communication media and storage media. To achieve both a program executing function and a function of dealing with AV (Audio/Video) stream data

25 on a high order, the data processing apparatus has a multimedia bus 200 in addition to an ordinary internal bus (Async Bus) 100 which executes event-driven type

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System Structure

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computation routine and so forth. The CPU interface 14 is a host bus bridge which bidirectionally connects the CPU bus and the internal bus 100. An I/O controller 22C is connected to the internal bus 100, and has various interfaces including an interface for outputting digital video signals to an external AV machine or the like and other interfaces for communication with various kinds of peripheral devices (an SIO interface, an I²C bus interface, an IR (Infrared) interface, a USB interface, an IDE interface and an MIDI interface). Storage devices such as a DVD drive and an HDD are connected to the I/O controller 22 via the IDE interface.

As illustrated, a multimedia bus manager 15, a media processor 16, a CAS module 18, a PCMCIA interface 19, and an IEEE1394 interface 21 are connected to the multimedia bus 200. Those multimedia bus manager 15, media processor 16, CAS module 18, PCMCIA interface 19 and IEEE1394 interface 21 are nodes (devices) each of which performs data transfer via the multimedia bus 200 and can use the aforementioned band-guaranteed cycle and asynchronous transfer cycle.

The multimedia bus manager 15 is the manager node for the multimedia bus 200, and performs control to execute the band-guaranteed cycle and asynchronous transfer cycle on the multimedia bus 200. Specifically, the multimedia bus manager 15 manages a reserved band,

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5 to the receiver node in peer-to-peer mode in the
aforementioned band-guaranteed cycle. The media
processor 16 performs, in parallel, a process of
decoding the MPEG-2 transport stream and reproducing
and displaying the decoded stream and a ciphering to
0 protect the MPEG-2 transport stream from an

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5. A specific transfer control scheme for the multimedia bus 200 will now be discussed.

1) Cycle time

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In the stream access, a sender node and a receiver node are designated for each channel and no other addresses than the channel are used. Wait control from the receiver side as in an ordinary PCI bus transaction is not carried out either. How this stream access is done is illustrated in FIG. 3. In FIG. 3, a node A is the sender node with the channel number 1 and a node D is the receiver node with the channel number 1. In this case, the nodes A and D to both of which the channel number 1 is assigned are logically connected on the multimedia bus 200 in a peer-to-peer fashion, and data transfer between the nodes A and D is directly carried out. For a single sender node, a plurality of receiver nodes with the same channel number as that of

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b) Single Access

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c) Burst access

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Channel Control Register

FIG. 4 shows the contents of a channel control register provided in each node on the multimedia

node.

A signal line (Disconnect) defined on the multimedia bus 200 is used for the flow control. Each node is connected to the signal line (Disconnect) in a wired OR fashion. When stream access is executed by the multi-cast, if one of the plurality of receiver nodes for the multi-cast makes the signal line active, the transmission of stream data from the sender node is forcibly stopped.

The principle of the flow control in a reserved band cycle will be explained referring to FIGS. 5A and 5B. FIG. 5A presents a timing chart for a case where a stream access of channel number 1 (Ch. 1) is carried out using a reserved band cycle of three time slots (TS1, TS2, TS3). When a disconnect signal (Disconnect) is asserted on the multimedia bus 200 by the receiver node during execution of the reserved band cycle, as shown in FIG. 5B, the sender node stops the current stream access and interrupts transmission of stream data in response to the disconnect signal. The disconnect signal (Disconnect) represents the completion of the current transfer cycle. When the next cycle time comes, the sender node restarts the interrupted stream access for transmitting subsequent stream data.

The provision of this scheme of stopping a stream access under the control of the receiver node,

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particularly the stopping of multi-cast transfer using a band-guarantee cycle in response to an instruction from any receiver node, can prevent the buffer of the receiver node from overflowing even when such

5 overflowing is likely to occur due to a delay in the
stream processing and reception of a variable bit rate
stream. It is therefore possible to efficiently
execute the required real-time transfer only with the
least required buffer.

10 FIG. 6 specifically shows timing for the flow
control.

First, signal lines included in the multimedia bus 200 will be explained. The multimedia bus 200 includes a clock signal (CLK) line, a 3-bit channel number/byte enable signal (ch_Num/BE) line, a 32-bit data (Data) line, a disconnect signal (Disconnect[—]) line, a bus request signal (Access REQ[—]) line, a bus grant signal (Access GNT[—]) line and a ready signal (Ready[—]) line. The upper line "[—]" represents an active-low signal.

20 The channel number/byte enable signal (ch_Num/BE)
indicates the channel number (Ch.) whose stream access
is to be started at the address phase of reserved band
cycle, and indicates a valid byte lane of data on the
data line at the data phase of the reserved band cycle.
25 The channel number is output by the manager node in the
reserved band cycle but is output by a bus mater node
which has obtained a bus-using permission in the Async

cycle.

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The disconnect signal (Disconnect^-) is a signal to disconnect nodes from the current stream access and indicates the completion and switching of the current transfer cycle. To forcibly stop transmission of stream data from the sender node during stream access, the receiver node outputs this disconnect signal (Disconnect^-). As the disconnect signal (Disconnect^-) usually indicates the end of a stream access, the manager node outputs the disconnect signal (Disconnect^-).

The access request signal (Access REQ^-) and access grant signal (Access GNT^-) are used to manage the bus-using permission for the Async cycle. The paired request signal (Access REQ^-) and access grant signal (Access GNT^-) are provided between the manager node that performs bus management and each node. An access request (bus-using permission request) is made using the Access REQ^- signal. The node which wants to access the bus asserts the Access REQ^- . Arbitration of the access request is carried out by the manager node. This node is informed of access permission by the Access GNT^- , which is asserted at the same time as the assertion of Disconnect^- . The node that is requesting an access latches the Disconnect^- and Access GNT^- by the CLK and when the Disconnect^- is asserted, the node to which the Access GNT^- is asserted obtains the

bus-using permission (master node).

In a stream access, each node can receive and output data in accordance with the clock CLK when its own channel number is designated by the channel

5 number/byte enable signal (ch_Num/BE). The channel number is output from the rising edge of the third clock from the clock at which the Disconnect[—] signal (indicating the end of the access cycle) has been asserted, and is latched at the rising edge of the
10 fourth clock. Since, in the reserved band cycle, the manager node serves as the master, assertion of the Access REQ[—] that requests stream access is inhibited. In the stream access mode, no wait control by the Ready[—] signal is not performed.

15 When the capacity of the reception buffer becomes smaller during a stream access in the reserved band cycle, the receiver node asserts the disconnect signal (Disconnect[—]). Asserting the disconnect signal causes the sender node to stop stream transfer. As a result,
20 the stream access which is in underway is terminated (intermitted). Thereafter, as mentioned above, the channel number to be accessed next is output from the manager node at the rising edge of the third clock from the clock at which the disconnect signal (indicating
25 the end of the access cycle) has been asserted. When the next cycle time comes, the sender node, at which the transmission of stream data is stopped, restarts

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FIGS. 7A and 7B exemplify a hardware structure which accomplishes the flow control using the disconnect signal.

5 As shown in FIG. 7A, the reception section of each
node is provided with a FIFO buffer 111, a reception
circuit 112 and an overflow detection circuit 113. The
FIFO buffer 111 is an input/output buffer for
temporarily storing data that is exchanged via the
10 multimedia bus 200. At the time of reception, stream
data input via the multimedia bus 200 to the reception
circuit 112, and sequentially written in the FIFO
buffer 111. The stream data stored in the FIFO buffer
111 is read out and processed by an internal processing
15 circuit. The overflow detection circuit 113 detects if
the amount of data stored in the FIFO buffer 111 has
exceeded a predetermined threshold value. When the
amount of data stored in the FIFO buffer 111 has
exceeded the predetermined threshold value, the
20 disconnect signal is generated to prevent the FIFO
buffer 111 from overflowing. The nodes other than the
manager node are connected to the disconnect signal
line through an open-drain output buffer. The open-
drain type buffer drives the disconnect signal line
25 into an active-low state. The reason why the open-
drain buffer is used will be described in detail with
reference to FIG. 9.

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Since, in the foregoing embodiment, the disconnect signal line is so formed that it can be driven by any receiver node, a drive conflict occurs among signals of

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node in order to accelerate the speed of shift from the active-low state to the inactive-high state.

The disconnect de-assert acceleration circuit 151 monitors the disconnect signal line through the input buffer 153 and detects whether the disconnect signal line is asserted as active low at the timing of the rising edge of a clock CLK. When the circuit 151 detects that the disconnect signal line has asserted as active low, the disconnect de-assert acceleration circuit 151 drives the disconnect signal line into the inactive-high state for a give period of time (1CLK period) using the 3-state output buffer 152 in order to accelerate the speed of shift from the active-low state to the inactive-high state. The de-assert of the disconnect signal line (shift from "Low" to "High") can thus be accelerated, as compared with the shift from the "Low" to the state "High" caused by only the pull-up register R.

FIG. 10 shows control timing of the disconnect signal line at the time of flow control.

If an overflow is detected at any receive node during the multi-cast transfer, an output signal (Disconnect[—]) from the open-drain output buffer provided at the receiver node is switched from "high impedance (Hi-Z)" to "Low". The disconnect signal line is therefore switched from the inactive-high state set by the pull-up resistor R to the active-low state and

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The receiver node drives the disconnect signal line only for a period of a 1CLK cycle. After that, the output signal (Disconnect[—]) from the open-drain output buffer provided at the receiver node is returned to the "high impedance (Hi-Z)".

Another example of control timing for accelerating a shift of the disconnect signal line from the active-low state to the inactive-high state will now be described.

If an overflow is detected at any receiver node during the multi-cast transfer, the receiver node drives the disconnect signal line into the active-low state for the first 1CLK cycle period and then into the

the FIFO buffer 303 exceeds a predetermined threshold value. If the amount does, the circuit 304 generates an overflow detection signal. The overflow detection signal is supplied to the disconnect signal drive
5 circuit 305 and disconnect signal monitor circuit 306.

Upon receiving the overflow detection signal, the disconnect signal drive circuit 305 drives the disconnect signal line into the active-low state for the first 1CLK cycle period using the disconnect signal
10 output 3-state buffer 307, and then drives it into the inactive-high state for the next 1CLK cycle period.

The disconnect signal monitor circuit 306 monitors the disconnect signal line through the input buffer 308, when overflow detection signal is input. When the
15 circuit 306 detects that the disconnect signal line has asserted as the active-low state at the rising edge of a clock CLK, it sets the disconnect signal output 3-state buffer 307 in the high impedance state to inhibit the disconnect signal drive circuit 305 from driving
20 the disconnect signal line. If it is not detected that the disconnect signal line has asserted as the active-low state when the overflow detection signal is input, the monitor circuit 306 allows the disconnect signal drive circuit 305 to drive the disconnect signal line.

25 In the above arrangement, too, the problem of a drive conflict among signals of the plural receiver nodes can be resolved without decreasing the bus use

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efficiency.

According to the system of the present embodiment described above, the use of the bus 200 in which the band-guaranteed cycle is defined as a transfer mode
5 allows the band of stream data requiring a high degree of real time to be guaranteed. Usually data transfer cannot be intermitted during the band-guaranteed cycle; however, in the present invention, the transmission of stream data from the sender node can be stopped under
10 the control of the receiver node, even during the band-guaranteed cycle.

The multi-cast transfer using the band-guaranteed cycle can be stopped even in response to an instruction from any receiver node. The provision of this scheme
15 of stopping the multi-cast transfer of stream data under the control of the receiver node can prevent the buffer from overflowing even when such overflowing is likely to occur at any receiver node for the multi-cast due to a delay in the stream processing and reception
20 of a variable bit rate stream. It is therefore possible to efficiently execute the multi-cast transfer of stream data through the bus 200 only with the least required buffer.

The scheme of avoiding the problem of a drive
25 conflict among disconnect signals and the provision of the scheme of accelerating the de-assert of disconnect signals allow the flow control to be efficiently

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performed at the time of stream access by the multi-cast.

5 In the foregoing embodiment, the pull-up resistor R is connected to the disconnect signal line. However, it can be replaced with a pull-down resistor and, in this case, the disconnect signal line is driven into the active-high state by the open-drain output buffer of each node.

10 The system of the present embodiment can be used as a platform of various types of digital information device, such as set-top boxes, digital TVs and game machines as well as computers.

15 As described above, according to the present invention, the transfer of stream data, especially the multi-cast transfer can be performed on the bus with efficiency, and all the receiver nodes for the multi-cast transfer can be prevented from overflowing without providing any huge buffers.

20 Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as
25 defined by the appended claims and their equivalents.

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